

# ***ADS8371EVM***

## *User's Guide*

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It is important to operate this EVM within the input voltage range of  $\pm 6$  V and the output voltage range of 0 V and 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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# Read This First

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### ***About This Manual***

This users guide describes the characteristics, operation, and use of the ADS8371 16-bit, 750-kHz, parallel interface, analog-to-digital converter evaluation board. A complete circuit description, schematic diagram, and bill of materials are included.

### ***How to Use This Manual***

This document contains the following chapters:

- ☐ Chapter 1 – EVM Overview
- ☐ Chapter 2 – Analog Interface
- ☐ Chapter 3 – Digital Interface
- ☐ Chapter 4 – Power Supply Requirements
- ☐ Chapter 5 – Using the EVM
- ☐ Chapter 6 – ADS8371EVM BOM, Layout, and Schematic

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#### **Data Sheets:**

ADS8371  
REF1004-2.5  
SN74AHC138  
SN74AHC245  
SN74AHC1G04  
THS4031  
OPA627

#### **Literature Number:**

SLAS390  
SBVS002  
SCLS258  
SCLS230  
SCLS318  
SLOS224  
SBOS165

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# **EVM Overview**

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This chapter contains the features of the ADS8371EVM.

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## 1.1 Features

- ☐ Full-featured evaluation board for the high-speed ADS8371 16-bit, single channel, parallel interface, SAR-type analog-to-digital converters.
- ☐ Onboard signal conditioning
- ☐ Onboard reference
- ☐ Input and output digital buffer
- ☐ Onboard decoding for stacking multiple EVMs

# Analog Interface

The ADS8371 analog-to-digital converter has both a positive and negative analog input pin. Ground for the negative input is provided on the EVM (via SJP7) close the device, or a user-furnished ground wire may be attached. The negative input pin has a range of –200 mV up to 200 mV, and is shorted on the EVM via SJP7. A signal for the positive input pin can be applied at connector P1, pin 2 (shown in Table 2–1 ), or applied to the center pin of SMA connector J1.

*Table 2–1. Analog Input Connector*

| Description        | Signal Name | Connector.Pin# |       | Signal Name | Description                |
|--------------------|-------------|----------------|-------|-------------|----------------------------|
| Pin tied to Ground | AGND        | P1.1           | P1.2  | +           | Noninverting Input Channel |
| Reserved           | N/A         | P1.3           | P1.4  | N/A         | Reserved                   |
| Reserved           | N/A         | P1.5           | P1.6  | N/A         | Reserved                   |
| Reserved           | N/A         | P1.7           | P1.8  | N/A         | Reserved                   |
| Pin tied to Ground | AGND        | P1.9           | P1.10 | N/A         | Reserved                   |
| Pin tied to Ground | AGND        | P1.11          | P1.12 | N/A         | Reserved                   |
| Reserved           | N/A         | P1.13          | P1.14 | N/A         | Reserved                   |
| Pin tied to Ground | AGND        | P1.15          | P1.16 | N/A         | Reserved                   |
| Pin tied to Ground | AGND        | P1.17          | P1.18 | N/A         | Reserved                   |
| Reserved           | N/A         | P1.19          | P1.20 | REF+        | External Reference Input   |

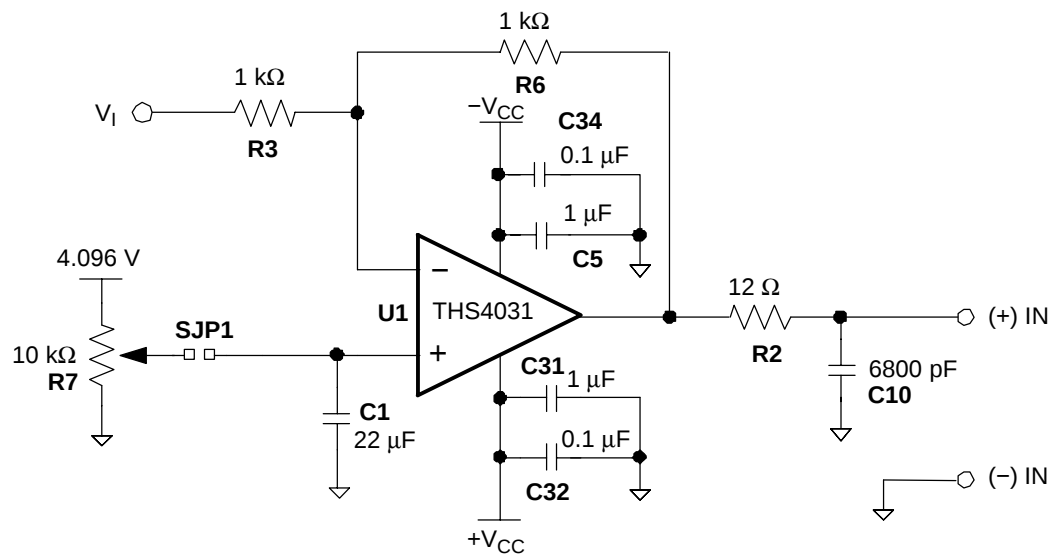
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## 2.1 Signal Conditioning

The factory recommends the analog input to any SAR-type converter be buffered and low-pass filtered. It is important to note that the input buffer circuit of the ADS8371EVM, shown in Figure 2–1, uses the THS4031 in an *inverting* gain-of-one configuration. The amplifier is not stable in a *conventional* gain-of-one configuration. The THS4031 was selected for its low noise, high slew rate, and fast settling time. The low-pass filter resistor and capacitor values are selected such that ADS8371EVM meets the 100-kHz AC performance specifications listed in the data sheet. The series resistor works with the capacitor to filter the input signal, but also isolates the amplifier from the 6800-pF capacitive load. The capacitor to ground at the input of the A/D works with the series resistor to filter the input signal, and acts like a charge reservoir. This external filter capacitor works with the amplifier to charge the internal sampling capacitor during sampling mode.

The EVM has a provision to offset the input voltage by adjusting R7, a 10-k $\Omega$  potentiometer.

Figure 2–1. Input Buffer Circuit



## 2.2 Reference

The ADS8371EVM allows users to select from two reference sources:

- ☐ an onboard (REF1004–2.5)
- ☐ a user supplied reference voltage via P1 pin 20

Both the user supplied reference and the onboard reference voltage can be amplified and filtered using reference amplifier, U2. The ADS8371EVM ships with the reference amplifier, U2, set for a gain of 1.6 V. The onboard reference (U10) is a 2.5-V reference. The user has the option of applying it directly to the converter, or routing the voltage through the reference amplifier. The ADS8371 has a onboard reference buffer, so it is not necessary to buffer the reference voltage being connecting it to the converter. Also, keep in mind that wiring the voltage reference through the amplifier gains the 2.5-V reference up to 4.096 V.

The ADS8371EVM ships with 4.096 V connected to the reference pin of the converter. See Chapter 6 for a full schematic and Table 2–2 for jumper settings.

*Table 2–2. Solder Short Jumper Setting*

| Reference Designator | Description                                   | Jumper Setting         |                        |
|----------------------|-----------------------------------------------|------------------------|------------------------|
|                      |                                               | 1–2                    | 2–3                    |
| SJP1                 | Apply offset voltage to A/D buffer            | Installed <sup>†</sup> | N/A                    |
| SJP2                 | Set amplifier U1 negative supply to ground    |                        |                        |
|                      | Set amplifier U1 negative supply to $-V_{CC}$ |                        | Installed <sup>†</sup> |
| SJP3                 | Set amplifier U2 negative supply to ground    |                        |                        |
|                      | Set amplifier U2 negative supply to $-V_{CC}$ |                        | Installed <sup>†</sup> |
| SJP4                 | Select internal reference source              | N/A                    |                        |
|                      | Select external reference voltage             |                        | Installed <sup>†</sup> |
| SJP5                 | Select onboard reference source               | Installed <sup>†</sup> |                        |
|                      | Select buffered reference source              |                        |                        |
| SJP6                 | Select onboard reference source               | Installed <sup>†</sup> |                        |
|                      | Buffer user supplied reference voltage        |                        |                        |
| SJP7                 | Short (–)IN pin to ground                     | Installed <sup>†</sup> | N/A                    |

<sup>†</sup> Factory-set condition

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## Digital Interface

The ADS8371EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient dual-row-header/socket combination at P2 and P3. Consult Samtec at [www.samtec.com](http://www.samtec.com) or 1-800-SAMTEC-9 for a variety of mating connector options.

Table 3–1. Pinout for Parallel Control Connector P2

| Connector.Pin | Signal              | Description                                                                |
|---------------|---------------------|----------------------------------------------------------------------------|
| P2.1          | $\overline{DC\_CS}$ | Daughtercard Board Select pin                                              |
| P2.3          |                     |                                                                            |
| P2.5          |                     |                                                                            |
| P2.7          | A0                  | Address line from processor                                                |
| P2.9          | A1                  | Address line from processor                                                |
| P2.11         | A2                  | Address line from processor                                                |
| P2.13         |                     |                                                                            |
| P2.15         |                     |                                                                            |
| P2.17         |                     |                                                                            |
| P2.19         | $\overline{INTC}$   | Set jumper W4 to select BUSY or inverted signal to be applied to this pin. |

**Note:** All even-numbered pins of P2 are tied to DGND.

Read ( $\overline{RD}$ ) and conversion start ( $\overline{CONVST}$ ) signals to the converter can be assigned to two different addresses in memory via jumper settings. This allows for the stacking of up to two ADS8371EVMs into processor memory. See Table 3–2 for jumper settings. Note, the evaluation module does not allow the chip select ( $\overline{CS}$ ) line of the converter to be assigned to different memory locations. It is therefore suggested that the  $\overline{CS}$  line be grounded or wired to an appropriate signal of the processor.

Table 3–2. Jumper Settings

| Reference Designator | Description                                       | Jumper Settings        |                        |
|----------------------|---------------------------------------------------|------------------------|------------------------|
|                      |                                                   | 1–2                    | 2–3                    |
| W1                   | Connect +5 VD from connector to +BVDD             | Installed <sup>†</sup> |                        |
|                      | Connect +3.3 VD from connector to +BVDD           |                        |                        |
| W2                   | Set A[2..0] = 0x1 to generate <i>RD</i> pulse     | Installed <sup>†</sup> |                        |
|                      | Set A[2..0] = 0x2 to generate <i>RD</i> pulse     |                        |                        |
| W3                   | Set A[2..0] = 0x3 to generate <i>convst</i> pulse | Installed <sup>†</sup> |                        |
|                      | Set A[2..0] = 0x4 to generate <i>convst</i> pulse |                        |                        |
| W4                   | Set inverted <i>BUSY</i> pulse                    |                        |                        |
|                      | Set <i>BUSY</i> pulse to <i>INTC#</i>             |                        | Installed <sup>†</sup> |

<sup>†</sup> Factory-set condition

The data bus is available at connector P3; see Table 3–3 for pinout information.

Table 3–3. Data Bus Connector P3

| Connector.Pin | Signal | Description                |
|---------------|--------|----------------------------|
| P3.1          | D0     | Buffered Data Bit 0 (LSB)  |
| P3.3          | D1     | Buffered Data Bit 1        |
| P3.5          | D2     | Buffered Data Bit 2        |
| P3.7          | D3     | Buffered Data Bit 3        |
| P3.9          | D4     | Buffered Data Bit 4        |
| P3.11         | D5     | Buffered Data Bit 5        |
| P3.13         | D6     | Buffered Data Bit 6        |
| P3.15         | D7     | Buffered Data Bit 7        |
| P3.17         | D8     | Buffered Data Bit 8        |
| P3.19         | D9     | Buffered Data Bit 9        |
| P3.21         | D10    | Buffered Data Bit 10       |
| P3.23         | D11    | Buffered Data Bit 11       |
| P3.25         | D12    | Buffered Data Bit 12       |
| P3.27         | D13    | Buffered Data Bit 13       |
| P3.29         | D14    | Buffered Data Bit 14       |
| P3.31         | D15    | Buffered Data Bit 15 (MSB) |

**Note:** All even-numbered pins of P3 are tied to DGND.

This evaluation module provides direct access to all the analog-to-digital converter control signals via connector J2; see Table 3–4.

Table 3–4. Pinout for Converter Control Connector, J2

| Connector.Pin | Signal              | Description                                                     |
|---------------|---------------------|-----------------------------------------------------------------|
| J2.1          | $\overline{CS}$     | Chip Select pin. Active low                                     |
| J2.3          | $\overline{RD}$     | Read pin. Active low                                            |
| J2.5          | $\overline{CONVST}$ | Convert start pin. Active low                                   |
| J2.7          | BYTE                | Byte select input. Used for 8-bit bus reading.                  |
| J2.9          | N/C                 | Not Connected                                                   |
| J2.11         | BUSY                | Converter status output. High when a conversion is in progress. |

**Note:** All even-numbered pins of J2 are tied to DGND.

# Power Supply Requirements

The EVM accepts four power supplies.

- ☐ A dual  $\pm V$ s DC supply for the dual supply op amps. Recommend a  $\pm 6$ -VDC supply.
- ☐ A single +5.0-VDC supply for analog section of the board (A/D + Reference).
- ☐ A single +5.0-V or +3.3-VDC supply for digital section of the board (A/D + address decoder + buffers).

There are two ways to provide these voltages.

- 1) Wire in the voltages at test points on the EVM. See Table 4–1.

*Table 4–1. Power Supply Test Points*

| Test Point | Signal | Description                                                |
|------------|--------|------------------------------------------------------------|
| TP12       | +BVDD  | Apply +3.3 V or +5.0 V. See ADC data sheet for full range. |
| TP10       | DGND   | Digital ground                                             |
| TP9        | +AVCC  | Apply +5.0 V.                                              |
| TP5        | +VA    | Apply +6.0 V. Positive supply for amplifier.               |
| TP3        | –VA    | Apply –6.0 V. Negative supply for amplifier.               |
| TP4        | AGND   | Analog ground                                              |

- 2) Use the power connector J3, and derive the voltages elsewhere. The pinout for this connector is shown below. If using this connector, set the W1 jumper to connect +3.3 V or +5 V from connector to +BVDD. Short W1 between pins 1–2 to select +5 VD, or short between pins 2–3 to select +3.3 VD as the source for the digital buffer voltage supply (+BVDD).

*Table 4–2. Power Connector, J3, Pinout*

| Signal     | Power Connector – J1 |    | Signal     |
|------------|----------------------|----|------------|
| +VA (+6 V) | 1                    | 2  | –VA (–6 V) |
| +5 VA      | 3                    | 4  | N/C        |
| DGND       | 5                    | 6  | AGND       |
| N/C        | 7                    | 8  | N/C        |
| +3.3 VD    | 9                    | 10 | +5 VD      |

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# Using the EVM

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The ADS8371EVM serves three functions

- 1) As a reference design
- 2) As a prototype board and
- 3) As software test platform

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## 5.1 As a Reference Board

As a reference design, the ADS8371EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The EVM analog input circuit is optimized for a 100-kHz sine wave; therefore, users may need to adjust the resistor and capacitor values of the A/D input RC circuit. In AC type applications where signal distortion is a concern, polypropylene capacitors should be used in the signal path.

## 5.2 As a Prototype Board

As a prototype board, the buffer circuit consists of a standard 8-pin SOIC footprint and resistor pads for inverting and noninverting configurations. The ADS8371EVM can be used to evaluate both dual-supply and single-supply amplifiers. The EVM comes installed with a dual-supply amplifier as it allows the user to take advantage of the full input voltage range of the converter. For applications that require single-supply operation (and a smaller input voltage range), the THS4031 can be replaced with a single-supply amplifier like the OPA300. Pad jumper SJP2 should be shorted between pads 1 and 2, as it shorts the minus supply pin of the amplifier to ground. Positive supply voltage can be applied via test point TP5 or connector J3, pin 1.

## 5.3 As a Software Test Platform

As a software test platform, connectors P1, P2, and P3 plug into the parallel interface connectors of the 5–6K interface card. The 5–6K interface card sits on the TMS320C5000™ and TMS320C6000™ DSP platform starter kit (DSK). The ADS8371EVM is then mapped into the processor memory space. This card also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS8371 analog-to-digital converter. See the 5–6K interface card user's guide (SLAU104) for more information.

For the software engineer, the ADS8371EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-inch headers and sockets to wire into prototype boards. The user need only provide 3 address lines (A2, A1, and A0) and address-valid line ( $\overline{DC\_CS}$ ) to connector P2. To choose the address combinations that generate  $\overline{RD}$  and  $\overline{CONVST}$ , set jumpers as shown in Table 3–2. Recall that the chip select ( $\overline{CS}$ ) signal is not memory-mapped or tied to P2; therefore, it must be controlled via a general purpose pin or shorted to ground at J2 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus via P3 and to control via J2.

# ADS8371EVM BOM, Layout, and Schematic

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This chapter contains the ADS8371EVM bill of materials, the layouts, and the schematic.

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## 6.1 ADS8371EVM Bill of Materials

Table 6–1 contains a complete bill of materials for the ADS8371EVM. The schematic diagram also is provided for reference. Contact the Product Information Center or send an e-mail to [dataconvapps@list.ti.com](mailto:dataconvapps@list.ti.com) for questions regarding this EVM.

Table 6–1. ADS8371EVM Bill Of Materials

| QTY | Value        | Reference Designators              | Footprint    | Mfg                          | Mfg's Part Number | Description                            |
|-----|--------------|------------------------------------|--------------|------------------------------|-------------------|----------------------------------------|
| 3   | NI           | R1 R2 R4                           | 805          | NOT INSTALLED                | NOT INSTALLED     | 1/16W 0603 Chip Resistor               |
| 2   | 1k           | R3 R6                              | 805          | Panasonic – ECG or Alternate | ERJ-6ENF1001V     | RES 1.00K $\Omega$ 1/10W 1% 0805 SMD   |
| 2   | 0            | R5 R13                             | 603          | Panasonic – ECG or Alternate | ERJ-3GEY0R00V     | RES 0 $\Omega$ 1/16W 5% 0603 SMD       |
| 1   | 10k          | R7                                 | BOURNS_32X4W | Bourns                       | 3214W-1-103E      | TRIMPOT 10 k $\Omega$ 4MM TOP ADJ SMD  |
| 1   | 1.2k         | R8                                 | 603          | Yageo America or Alternate   | 9C06031A1201FKHFT | RES 1.20 k $\Omega$ 1/10W 1% 0603 SMD  |
| 1   | 0            | R9                                 | 805          | Panasonic – ECG or Alternate | ERJ-6GEY0R00V     | RES 0.0 $\Omega$ 1/10W 5% 0805 SMD     |
| 1   | 100          | R10                                | 603          | Panasonic – ECG or Alternate | ERJ-3EKF1000V     | RES 100 $\Omega$ 1/16W 1% 0603 SMD     |
| 1   | 768          | R11                                | 603          | Panasonic – ECG or Alternate | ERJ-3EKF7680V     | RES 768 $\Omega$ 1/16W 1% 0603 SMD     |
| 1   | 12           | R12                                | 805          | Panasonic – ECG or Alternate | ERJ-6GEYJ120V     | RES 12 $\Omega$ 1/8W 5% 0805 SMD       |
| 1   | 49.9         | R14                                | 805          | Panasonic – ECG or Alternate | ERJ-6ENF49R9V     | RES 49.9 $\Omega$ 1/10W 1% 0805 SMD    |
| 1   | 49.9k        | R15                                | 805          | Panasonic – ECG or Alternate | ERJ-6ENF4992V     | RES 49.9 k $\Omega$ 1/10W 1% 0805 SMD  |
| 4   | 10k          | R16 R17 R18 R19                    | 603          | Panasonic – ECG or Alternate | ERJ-3EKF1002V     | RES 10.0 k $\Omega$ 1/16W 1% 0603 SMD  |
| 1   | 10k          | R20                                | 805          | Panasonic – ECG or Alternate | ERA-S15J103V      | RES 10 k $\Omega$ 1/10W 1500PPM 5%0805 |
| 1   | 22 $\mu$ F   | C1                                 | 805          | TDK Corporation or Alternate | C2012X5R0J226M    | CAP CER 22 $\mu$ F 6.3V X5R 20% 0805   |
| 3   | NI           | C2 C3                              | 805          | NOT INSTALLED                | NOT INSTALLED     | 1/16W 0603 chip resistor               |
| 7   | 0.1 $\mu$ F  | C4 C25 C32 C34 C40 C48 C58         | 805          | Kemet or Alternate           | C0805C104J5RACTU  | CAP 0.10 $\mu$ F 50V ceramic X7R 0805  |
| 4   | 1 $\mu$ F    | C5 C6 C31 C41                      | 805          | Panasonic – ECG or Alternate | ECJ-GVB1C105K     | CAP 1 $\mu$ F 16V ceramic X5R 0805     |
| 1   | 6800 pF      | C10                                | TH           | WIMA                         | FKP2 6800/100/1   | 6800 pF polypropylene capacitor        |
| 3   | NI           | C7 C46 C47                         | 603          | NOT INSTALLED                | NOT INSTALLED     |                                        |
| 1   | NI           | C8                                 | TH           | NOT INSTALLED                | NOT INSTALLED     |                                        |
| 9   | 0.01 $\mu$ F | C9 C17 C18 C20 C24 C51 C52 C54 C56 | 603          | Kemet or Alternate           | C0603C103J5RACTU  | CAP 10000 pF 50V ceramic X7R 0603      |

| QTY | Value           | Reference Designators                                                 | Footprint    | Mfg                          | Mfg's Part Number | Description                                                                |
|-----|-----------------|-----------------------------------------------------------------------|--------------|------------------------------|-------------------|----------------------------------------------------------------------------|
| 1   | 10 $\mu$ F      | C11                                                                   | 3528         | Kemet or Alternate           | T491B106K016AS    | Capacitor TANT 10 $\mu$ F 16V 10% SMT                                      |
| 13  | 0.1 $\mu$ F     | C12 C13<br>C14 C19<br>C21 C22<br>C23 C26<br>C50 C53<br>C60 C61<br>C62 | 603          | Kemet or Alternate           | C0603C104K3RACTU  | CAP 0.1 $\mu$ F 25 V ceramic X7R 0603                                      |
| 1   | 0.47 $\mu$ F    | C15                                                                   | 603          | Panasonic – ECG or Alternate | ECJ-1VF1C474Z     | CAP 0.47 $\mu$ F 16 V ceramic Y5V 0603                                     |
| 2   | 0.01 $\mu$ F    | C28 C36                                                               | 1206         | Kemet or Alternate           | C1206C103J5RACTU  | CAP 10000 pF 50 V ceramic X7R 1206                                         |
| 2   | 0.01 $\mu$ F    | C49 C57                                                               | 805          | Kemet or Alternate           | C0805C103K5RACTU  | CAP 10000 pF 50 V ceramic X7R 0805                                         |
| 4   | 1000 pF         | C30 C37                                                               | 1206         | Kemet or Alternate           | C1206C102J5GACTU  | CAP 1000 pF 50 V ceramic NPO 1206                                          |
|     |                 | C45 C59                                                               |              |                              |                   |                                                                            |
| 2   | 1 $\mu$ F       | C29 C39                                                               | 1206         | Kemet or Alternate           | C1206C105K3RACTU  | CAP 1.0 $\mu$ F 25 V ceramic X7R 1206                                      |
| 4   | 10 $\mu$ F      | C16 C33<br>C38 C43                                                    | 1206         | Panasonic – ECG or Alternate | ECJ-3YB1C106M     | CAP 10 $\mu$ F 16 V ceramic X5R 1206                                       |
| 4   | 10 $\mu$ F      | C27 C35<br>C44 C55                                                    | 6032         | Panasonic – ECG or Alternate | ECS-T1EC106R      | CAP 10 $\mu$ F 25 V Tantalum TE SMD                                        |
| 1   | 47 $\mu$ F      | C42                                                                   | 1206         | TDK Corporation or Alternate | C3216X5R0J476M    | CAP CER 47 $\mu$ F 6.3 V X5R 20% 1206                                      |
| 1   | 100             | RP1                                                                   | CTS_742      | CTS Corporation              | 742C163101JTR     | RES array 100 $\Omega$ 16 TRM 8RES SMD                                     |
| 2   | 1K              | RP2 RP3                                                               | CTS_742      | CTS Corporation              | 742C163102JTR     | RES array 1 k $\Omega$ 16TERM 8RES SMD                                     |
| 4   | BLM21AJ601 SN1L | L1 L2 L3<br>L4                                                        | 1206         | Murata ERIE                  | BLM31PG601SN1L    | Chip ferrite beads - 600 $\Omega$ at 100 MHz                               |
| 1   | THS4031         | U1                                                                    | 8-SOP(D)     | Texas Instruments            | THS4031IDR        | 100 MHz low-noise high-speed amplifier                                     |
| 1   | OPA627          | U2                                                                    | 8-SOP(D)     | Texas Instruments            | OPA627AU          | Low-noise high-speed amplifier                                             |
| 1   | NI              | U3                                                                    | 3-SOT-23     | NOT INSTALLED                | NOT INSTALLED     | REF3040 50 ppm/ $^{\circ}$ C, 50 $\mu$ A in SOT23-3 CMOS voltage reference |
| 1   | ADS8371         | U4                                                                    | SOCKET_48QFP | Texas Instruments            | ADS8371IPFB       | ADS8371 16-Bit 750 KSPS                                                    |
| 3   | SN74AHC24 5PWR  | U5 U8 U9                                                              | 20-TSSOP(PW) | Texas Instruments            | SN74AHC245PWR     | Octal bus transceiver, 3-state                                             |
| 1   | SN74AHC1G 04DBV | U6                                                                    | 5-SOT(DBV)   | Texas Instruments            | SN74AHC1G04DBVR   | Single inverter gate                                                       |
| 1   | SN74AHC13 8PWR  | U7                                                                    | 16-TSSOP(PW) | Texas Instruments            | SN74AHC138PWR     | 3-Line to 8-line decoder/demultiplexer                                     |
| 1   | Reference Chip  | U10                                                                   | 8-SOP(D)     | Texas Instruments            | REF1004C-2.5      | 2.5 V micropower voltage reference                                         |
| 1   | SMA_PCB_MT      | J1                                                                    | SMA_JACK     | Johnson Components Inc.      | 142-0701-301      | Right angle SMA connector                                                  |

| QTY | Value                     | Reference Designators                      | Footprint                 | Mfg                  | Mfg's Part Number  | Description                            |
|-----|---------------------------|--------------------------------------------|---------------------------|----------------------|--------------------|----------------------------------------|
| 1   | 6X2X.1                    | J2                                         | 6X2X.1_SMT_PLUG_&_SOCKET  | Samtec               | TSM-106-01-T-D-V-P | 0.025" SMT plug – top side of PWB      |
| 1   | 5X2X.1                    | J3                                         | 5X2X.1_SMT_SOCKET         | Samtec               | SSW-105-22-S-D-VS  | 0.025" SMT socket – bottom side of PWB |
|     |                           |                                            |                           | Samtec               | TSM-105-01-T-D-V-P | 0.025" SMT plug – top side of PWB      |
| 2   | 10X2X.1                   | P1 P2                                      | 10X2X.1_SMT_PLUG_&_SOCKET | Samtec               | SSW-110-22-S-D-VS  | 0.025" SMT socket – bottom side of PWB |
|     |                           |                                            |                           | Samtec               | TSM-110-01-T-D-V-P | 0.025" SMT plug – top side of PWB      |
| 1   | 18X2X.1_SMT_PLUG_&_SOCKET | P3                                         | 16X2X.1_SMT_PLUG_&_SOCKET | Samtec               | SSW-116-22-S-D-VS  | 0.025" SMT socket – bottom side of PWB |
|     |                           |                                            |                           | Samtec               | TSM-116-01-T-D-V-P | 0.025" SMT plug – top side of PWB      |
| 4   | 3POS_JUMPER               | W1 W2 W3 W4                                | 3pos_jump                 | Samtec               | TSW-103-07-L-S     | 3 Position jumper 0.1" spacing         |
| 2   | SJP2                      | SJP1 SJP7                                  | SJP2                      | NOT INSTALLED        | NOT INSTALLED      | Pad 2 position jumper                  |
| 5   | SJP3                      | SJP2 SJP3 SJP4 SJP5 SJP6                   | SJP3                      | NOT INSTALLED        | NOT INSTALLED      | Pad 3 Position jumper                  |
| 10  | TP_.025                   | TP1 TP2 TP3 TP5 TP7 TP8 TP9 TP11 TP12 TP15 | test_point2               | Keystone Electronics | 5000K–ND           | Test point PC mini 0.040" D red        |
| 6   | TP_.025                   | TP4 TP10 TP6 TP16 TP13 TP14                | test_point2               | Keystone Electronics | 5001K–ND           | Test point PC mini 0.040" D black      |

## 6.2 ADS8371EVM Layout

Figure 6–1. Top Layer—Layer 1

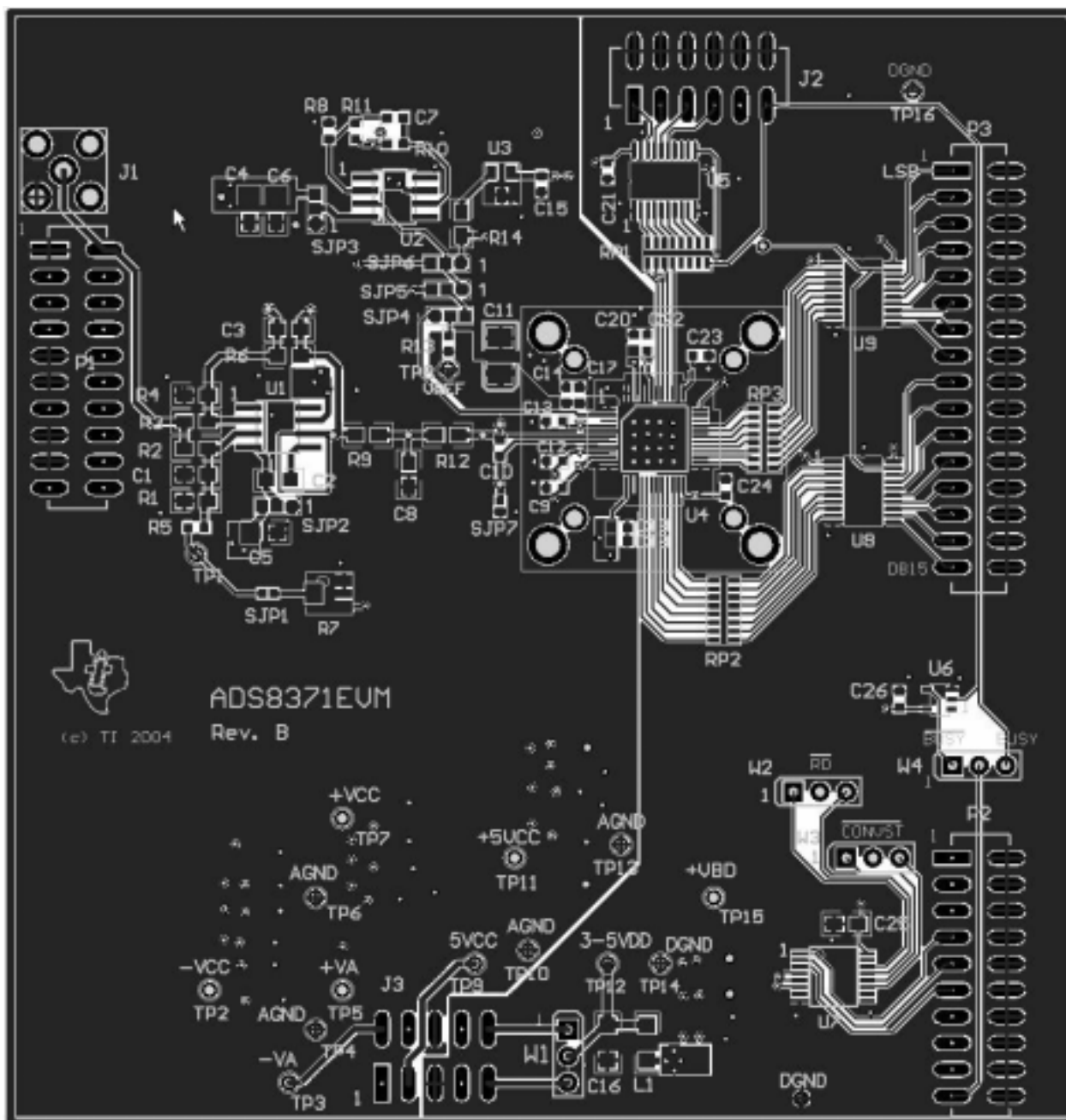


Figure 6-2. Ground Plane—Layer 2

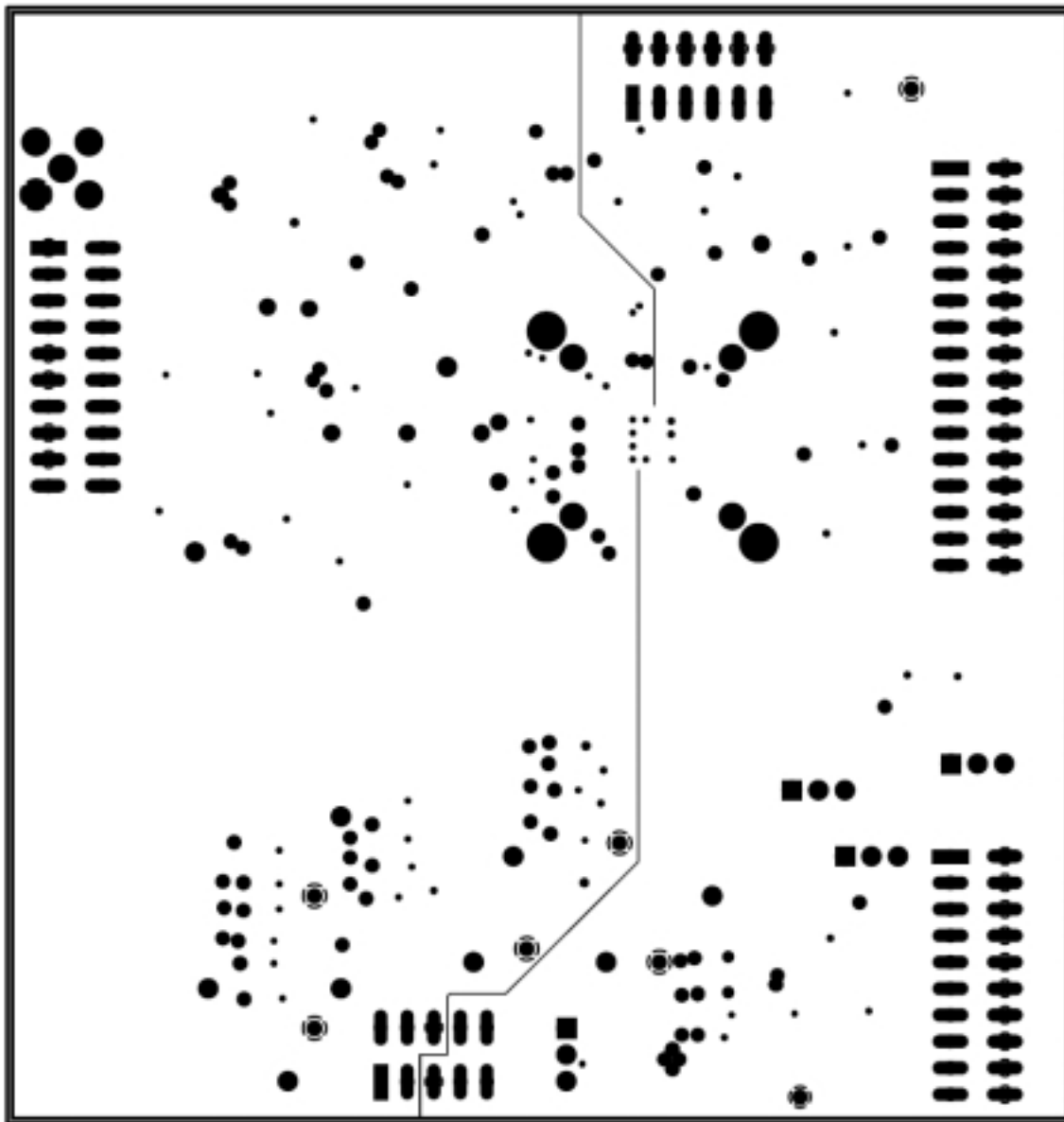


Figure 6-3. Power Plane—Layer 3

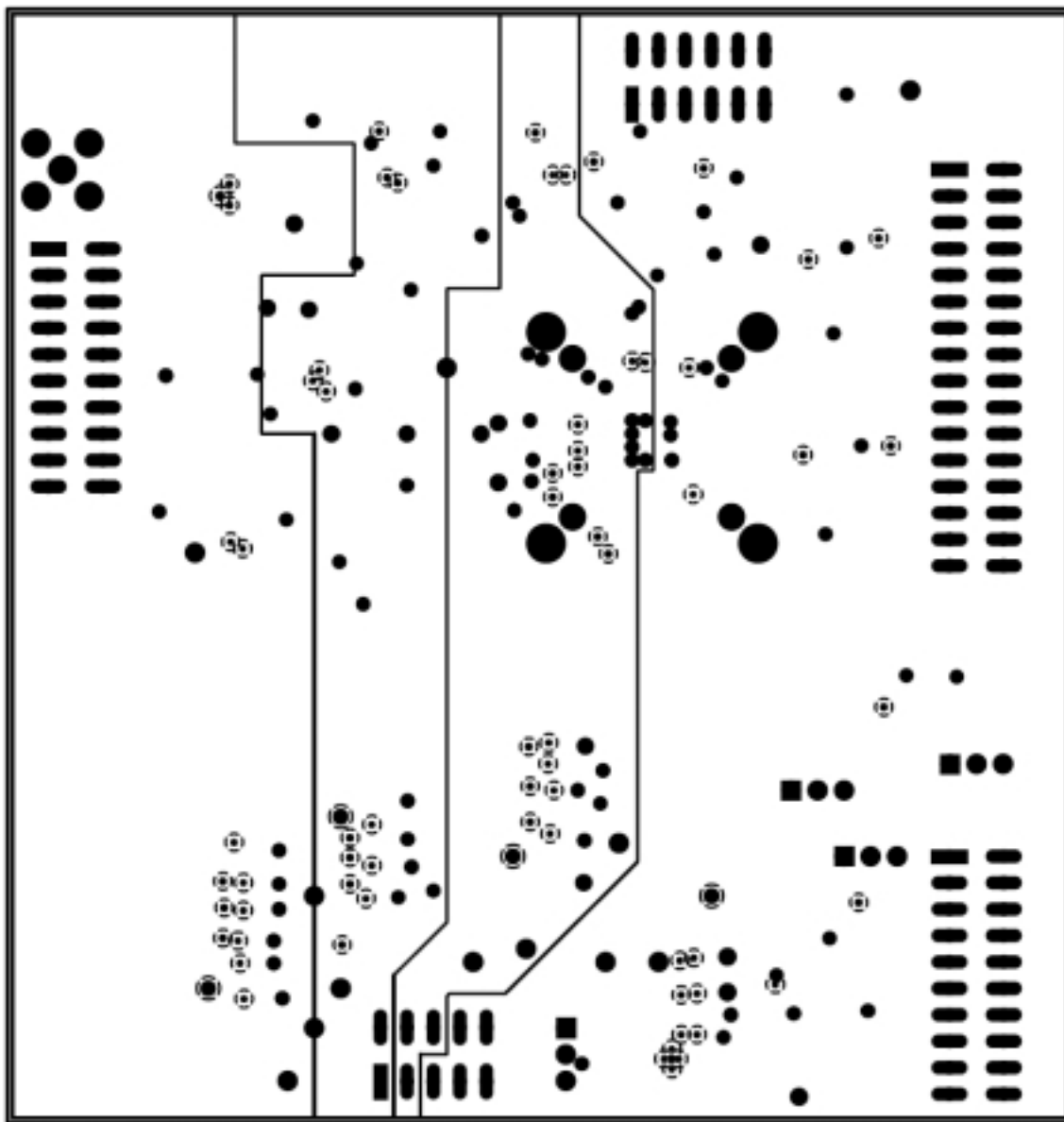
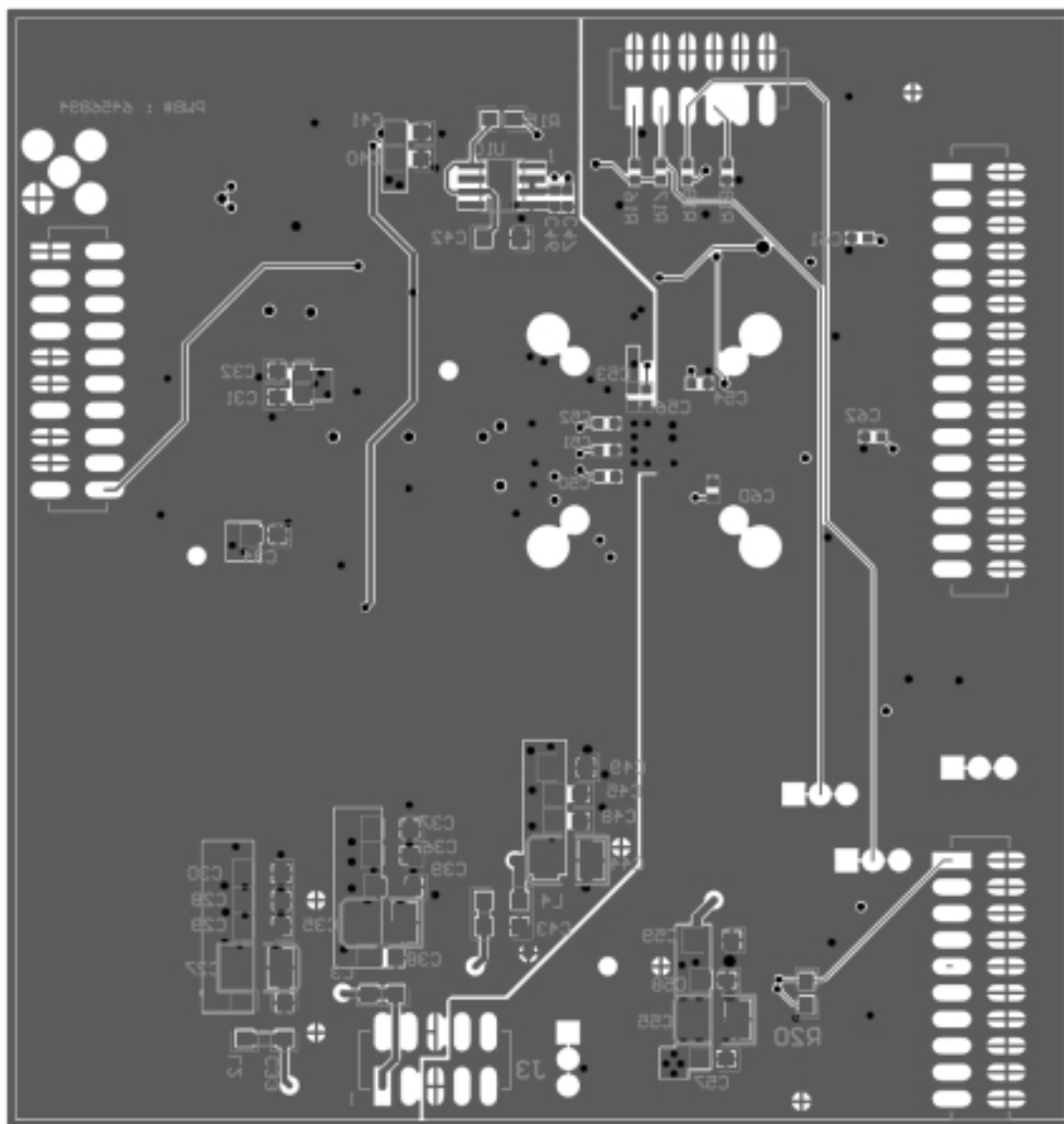
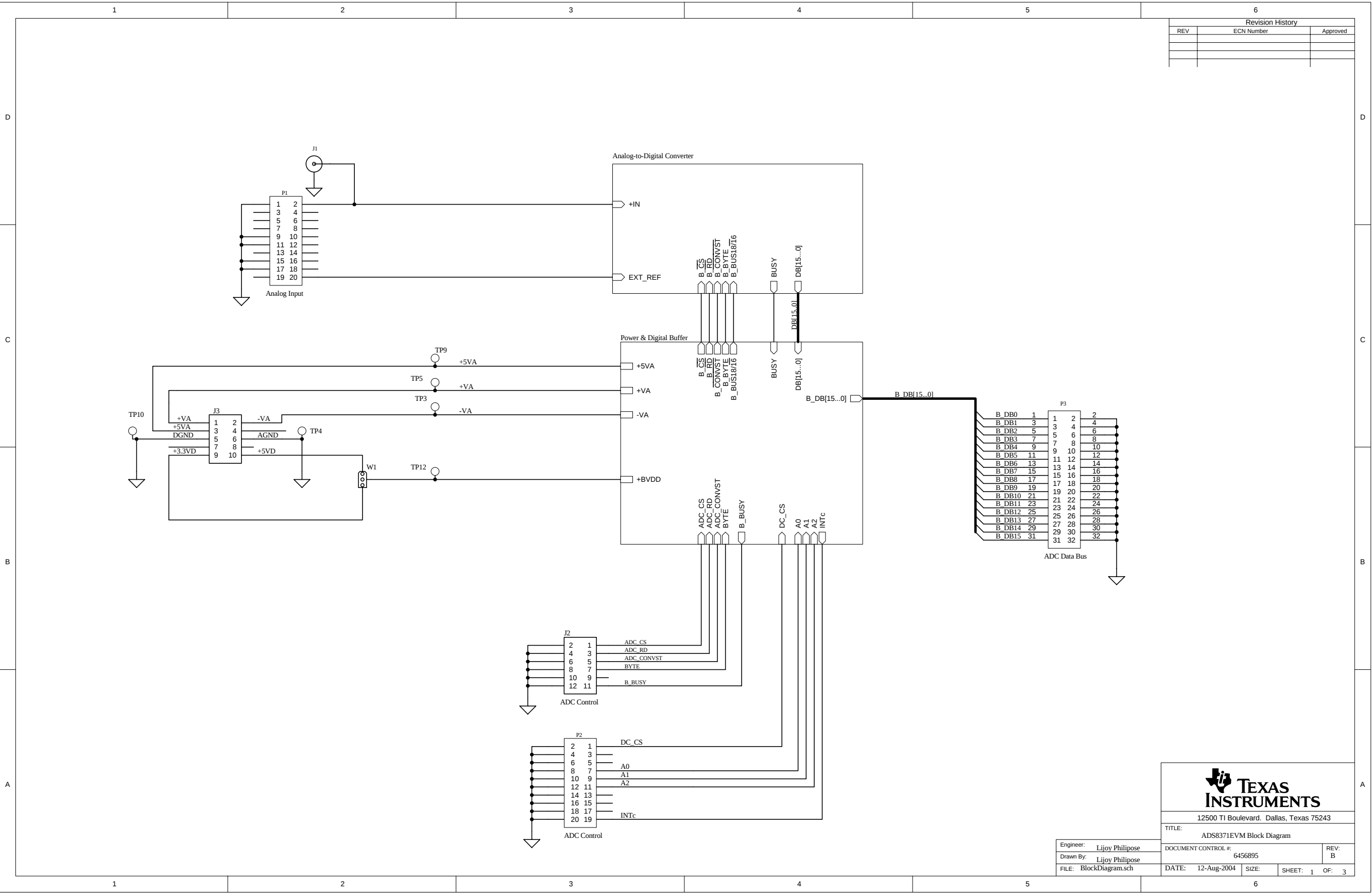


Figure 6–4. Bottom Layer—Layer 4



### 6.3 ADS8371EVM Schematic

The schematic follows this page.

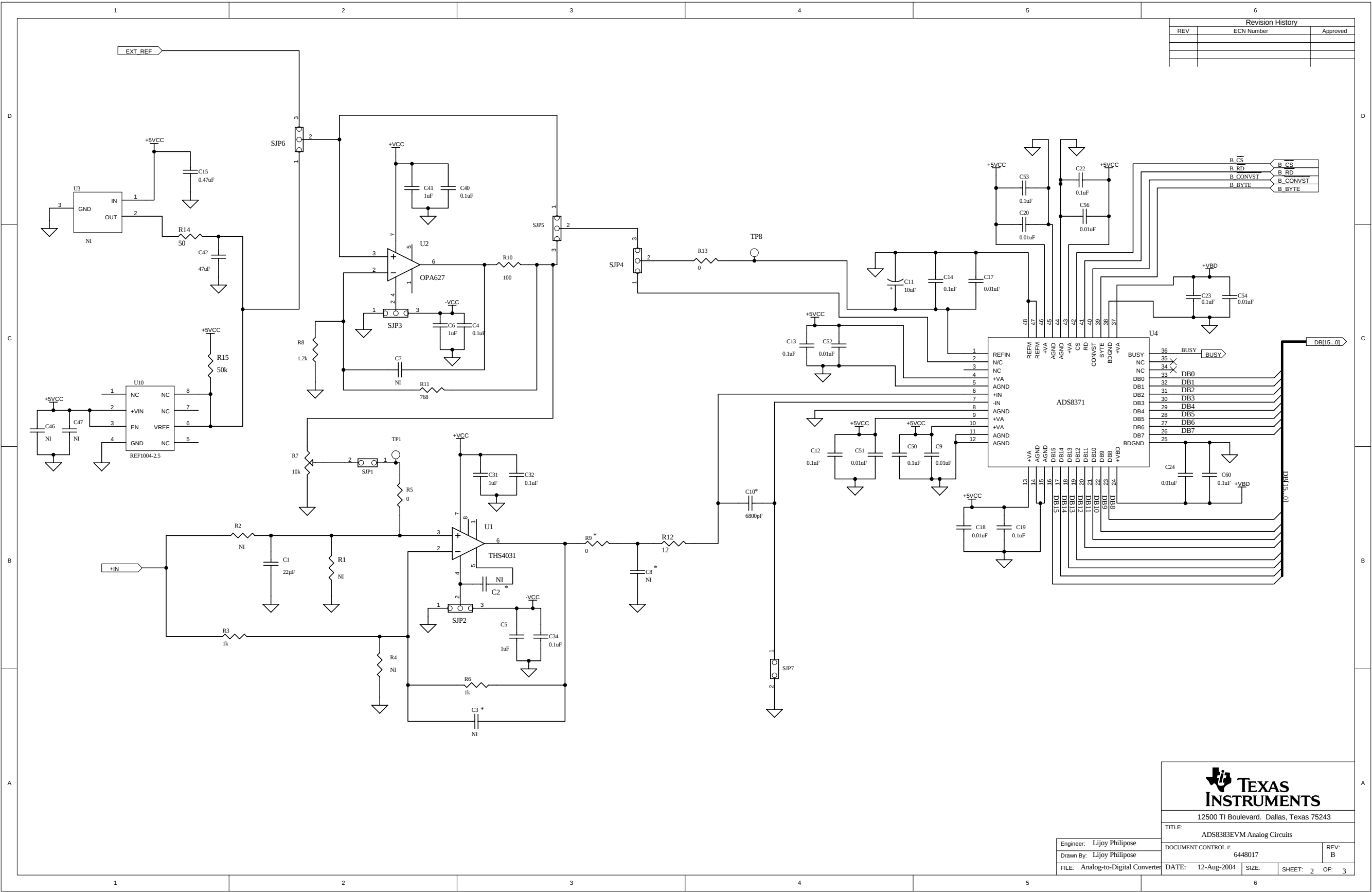


| Revision History |            |          |
|------------------|------------|----------|
| REV              | ECN Number | Approved |
|                  |            |          |
|                  |            |          |
|                  |            |          |



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|                                 |                             |                      |
|---------------------------------|-----------------------------|----------------------|
| TITLE: ADS8371EVM Block Diagram |                             |                      |
| Engineer: Lijoy Philipose       | DOCUMENT CONTROL #: 6456895 | REV: B               |
| Drawn By: Lijoy Philipose       | DATE: 12-Aug-2004           | SIZE: SHEET: 1 OF: 3 |
| FILE: BlockDiagram.sch          |                             |                      |



| Revision History |            |          |
|------------------|------------|----------|
| REV              | ECN Number | Approved |
|                  |            |          |
|                  |            |          |
|                  |            |          |



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|-----------------------------------|---------|----------------|
| TITLE: ADS8383EVM Analog Circuits |         |                |
| DOCUMENT CONTROL #:               | 6448017 | REV: B         |
| DATE: 12-Aug-2004                 | SIZE:   | SHEET: 2 OF: 3 |

Engineer: Lijoy Philipose  
Drawn By: Lijoy Philipose  
FILE: Analog-to-Digital Converter

